WHAT IS CLAIMED IS

1. A semiconductor package including a plurality of electrically-connected semiconductor chips, comprising:

a main semiconductor chip having a plurality of main chip pads and operating as a lead frame or a substrate;

a plurality of metal patterns electrically connected to each corresponding main chip pad and having electrodes formed on both ends;

one or more sub semiconductor chip adhered to the main semiconductor chip by adhering bumps formed on a plurality of sub chip pads to each corresponding electrode;

a dam formed on the main semiconductor chip in a shape surrounding the inner electrodes except for the outer electrodes on the outmost region of the main semiconductor chip;

filling materials filled up in the dam; and

a plurality of solder balls adhered on the outmost electrodes.

2. The semiconductor package according to claim 1, wherein the metal pattern comprises:

a lower barrier layer formed on the main chip pad;

a seed layer formed on the lower barrier layer;

and

a metal layer formed on the seed layer.

3. The semiconductor package according to claim 2, wherein the lower barrier layer comprises one selected from group consisting of Ti/W, Cr+Ni, Ti/W+Ni and Cr+Co+Ni, having a thickness of 2000 to 5000Å, the seed layer comprises one selected from group consisting of Cu, Au, Cr and Ni, having a thickness of 1 to 5㎛ and the metal layer is made of compounds such as Cu, Ni+Cu, Cu+Ni+Au or Cu+Au, having a thickness of 2 to 10㎛.

4. The semiconductor package according to claim 1, wherein the outer peripheral electrode and the inner electrode have a shape of circle, the inner electrode having a size of Ø0.1㎜ to Ø1㎜ and the outer peripheral electrode having a size of Ø0.3㎜ to Ø3㎜.

5. The semiconductor package according to claim 1, wherein the outer peripheral electrode and the inner electrode have a shape of rectangle, the inner electrode having a size of 0.1㎜×0.1㎜ to 1㎜×1㎜ and the outer peripheral electrode having a size of 0.3㎜× 0.3㎜ to 3㎜×

3mm.

6. The semiconductor package according to claim 1, wherein the bump comprises solder or gold.

7. The semiconductor package according to claim 1, wherein the dam comprises nonconductive polymer, having the same height to the adhered sub semiconductor chip.

8. The semiconductor package according to claim 1, wherein the filling material comprises nonconductive polymer.

9. The semiconductor package according to claim 1, wherein the solder ball adhered to the outer peripheral electrode is formed higher than the sub semiconductor chip by at least 0.1mm to 5mm.

10. A method of fabricating the semiconductor package comprising the steps of:

forming a plurality of metal patterns connected to each corresponding main chip pad on the main semiconductor chip operating as a lead frame or a substrate and having electrodes formed on both ends thereof;

forming a bump on each sub chip pad of sub

semiconductor chip;

adhering the sub semiconductor chip to the main semiconductor chip by adhering the bump to each corresponding electrode;

forming a dam on the main semiconductor chip in a shape surrounding inner electrodes except for outer electrodes on the outmost region of the main semiconductor chip and then, filling up the inside thereof with filling materials; and

adhering solder balls to the outmost electrodes.

11. The method of fabricating the semiconductor package according to claim 10, wherein the step of forming the metal pattern comprises the steps of:

sequentially forming a lower barrier material and a seed material on the entire surface of the main semiconductor chip;

forming a lower barrier layer and a seed layer on the main chip pad by selectively removing the lower barrier material and the seed material using an etch process;

forming an insulating layer on the region not having formed the lower barrier layer and the seed layer;

forming a metal layer on the entire surface of the main semiconductor chip;

forming a plurality of metal patterns having electrodes at both ends thereof by selectively removing the metal layer using an etch process; and

forming a protecting layer on the upper part of the metal layer except for electrodes at both ends.

12. The method of fabricating the semiconductor package according to claim 11, wherein the lower barrier layer comprises one selected from group consisting of Ti/W, Cr+Ni, Ti/W+Ni and Cr+Co+Ni, having a thickness of 2000 to 5000Å, the seed layer comprises one selected from group consisting of Cu, Au, Cr and Ni, having a thickness of 1 to 5㎛.

13. The method of fabricating the semiconductor package according to claim 11, wherein the insulating layer comprises nonconductive polyimide or polymer, having the same height to the seed layer.

14. The method of fabricating the semiconductor package according to claim 11, wherein the metal layer comprises one selected from group consisting of Cu, Ni+Cu, Cu+Ni+Au and Cu+Au, having a thickness of 2 to 10㎛.

15. The method of fabricating the semiconductor package according to claim 10, wherein the step of forming bump comprises the steps of:

sequentially forming a lower barrier material and a seed material on the entire surface of the sub semiconductor chip;

forming a lower barrier layer and a seed layer on the sub chip pad by selectively removing the lower barrier material and the seed material using an etch process;

forming a photoresist on the entire surface of the sub semiconductor chip to expose the upper part of the seed layer; and

forming a bump on the seed layer and removing the photoresist.

16. The method of fabricating the semiconductor package according to claim 15, wherein the lower barrier layer comprises one selected from group consisting of Ti/W, Cr+Ni, Ti/W+Ni and Cr+Co+Ni, having a thickness of 2000 to 5000Å, the seed layer comprises one selected from group consisting of Cu, Au, Cr and Ni, having a thickness of 1 to 5㎛.

17. The method of fabricating the semiconductor

package according to claim 15, wherein the bump comprises solder or gold.

18. The method of fabricating the semiconductor package according to claim 10, wherein the dam comprises nonconductive polymer, having the same height to the adhered sub semiconductor chip.

19. The method of fabricating the semiconductor package according to claim 10, wherein the filling material comprises nonconductive polymer.

20. The method of fabricating the semiconductor package according to claim 10, wherein the solder ball adhered to the outer peripheral electrode is formed higher than the sub semiconductor chip by at least 0.1mm to 5mm.